

## What is claimed is:

**[Claim 1]** A method of forming a resistor disposed on a substrate comprising the steps of:  
depositing a first seed layer of a first resistive material on said substrate with a first thickness and a first crystal structure;  
depositing a second layer of a second resistive material different from said first resistive material on said substrate with a second thickness and a second crystal structure such that said second crystal structure is controlled by said first crystal structure; and  
patterning said first and second layers of resistive material to define a resistor.

**[Claim 2]** A method according to claim 1, in which said first resistive material is selected from the group including TiN, Ta, Ti, W, WN, Al<sub>2</sub>O<sub>3</sub>, and TaO and said second resistive material is selected from the group including TaN, TiN, SiCr, WN and W.

**[Claim 3]** A method according to claim 2, in which said first thickness is less than 20% of said second thickness.

**[Claim 4]** A method according to claim 1, further comprising a step of patterning said first resistive material to form at least two pads; and  
said second layer of resistive material is not formed over at least a selected one of said at least two pads, whereby a single-layer resistor is formed from said selected one of said at least two pads.

**[Claim 5]** A method according to claim 3, further comprising a step of patterning said TiN to form at least two pads; and  
said TaN is not formed over at least a selected one of said at least two pads of TiN, whereby a single-layer resistor of TiN is formed from said selected one of said at least two pads.

**[Claim 6]** A method according to claim 1, in which said second resistive material is disposed in at least two locations, a first location disposed above said first layer of resistive material and a second location disposed directly on said substrate, whereby a single-layer resistor is formed from said second resistive material in said second location.

**[Claim 7]** A method according to claim 3, in which said TaN is disposed in at least two locations, a first location disposed above said TiN and a second location disposed directly on said substrate, whereby a single-layer resistor is formed from said TaN in said second location.

**[Claim 8]** A method according to claim 3, in which said second resistive material is disposed in at least three locations, a first location disposed above a pad of said first layer of resistive material and a second location disposed directly on said substrate, whereby a single-layer resistor is formed from said second resistive material in said second location, a single-layer resistor is formed from said first resistive material in said selected one of said at least two pads and a controlled structure resistor is formed from said second resistive material disposed above said first resistive material.

**[Claim 9]** A method according to claim 2, in which a TiN layer is deposited at a temperature between 40C and 100C in an argon: nitrogen mixture in the range 3:1 to 5:1.

**[Claim 10]** A method according to claim 2, in which a TaN layer is deposited at a temperature between 40C and 200C in an argon: nitrogen mixture in the range 1.5:1 to 3:1.

**[Claim 11]** A method of forming at least two types of resistors disposed on a substrate comprising the steps of:

depositing a first layer of a first resistive material on said substrate with a first thickness and a first crystal structure;

patterning said first layer of resistive material to form at least two pads;

depositing a second layer of a second resistive material different from said first resistive material on said substrate with a second thickness and a second crystal structure such that said second crystal structure is controlled by said first crystal structure and said second thickness is adapted to combine with said first thickness to generate a final sheet rho having a design value;

patterning said second layer of resistive material to remove said second layer of resistive material above at least one of said at least two pads, whereby a first type of resistor is formed from a bilayer of said first resistive material and said second resistive material and a second type of resistor is formed from said first resistive material only without said second resistive material.

**[Claim 12]** A method according to claim 11, in which said first resistive material is selected from the group including TiN, Ta, Ti, W, WN, Al<sub>2</sub>O<sub>3</sub>, and TaO and said second resistive material is selected from the group including TaN, TiN, SiCr, WN and W.

**[Claim 13]** A method according to claim 11, in which said step of patterning said second layer of resistive material comprises patterning an area of said second resistive material over a portion of said substrate that does not have a pad of said first resistive material, thereby forming a third type of resistor of said second resistive material without said first resistive material.

**[Claim 14]** An integrated circuit comprising at least one resistor of a first resistor type disposed on a substrate comprising:

a first layer of a first resistive deposited on said substrate with a first thickness and a first crystal structure;

a second layer of a second resistive material different from said first resistive material deposited on said substrate above at least said first layer of resistive material with a second thickness and a second crystal structure such that said second crystal structure is controlled by said first crystal structure and said second thickness is adapted to combine with said first thickness to generate a final TCR having a design value.

**[Claim 15]** An integrated circuit according to claim 14, in which said first resistive material is selected from the group including TiN, Ta, Ti, W, WN, Al<sub>2</sub>O<sub>3</sub>, and TaO and said second resistive material is selected from the group including TaN, TiN, SiCr, WN and W.

**[Claim 16]** An integrated circuit according to claim 14, in which said first thickness is less than 20% of said second thickness.

**[Claim 17]** An integrated circuit according to claim 14, further comprising a second resistor of a second resistor type comprising a single layer of said first resistive material.

**[Claim 18]** An integrated circuit according to claim 14, further comprising a resistor of a third resistor type comprising a single layer of said second resistive material.

**[Claim 19]** An integrated circuit according to claim 16, further comprising a resistor of a third resistor type comprising a single layer of said second resistive material, whereby said integrated circuit includes a bilayer resistor and two types of single layer resistor.

**[Claim 20]** An integrated circuit according to claim 16, in which said first resistive material is selected from the group including TiN, Ta, Ti, W, WN, Al<sub>2</sub>O<sub>3</sub>, and TaO and said second resistive material is selected from the group including TaN, TiN, SiCr, WN and W.